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Phase qubits fabricated with trilayer junctions

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Abstract

We have developed a novel Josephson junction geometry with minimal volume of lossy isolation dielectric, suitable for higher quality trilayer junctions implemented in qubits. The junctions are based on *in situ* deposited trilayers with thermal tunnel oxide, have micron-sized areas and a low subgap current. In qubit spectroscopy only a few avoided level crossings are observed, and the measured relaxation time of $T_1 \approx 400$ ns is in good agreement with the usual phase qubit decay time, indicating low loss due to the additional isolation dielectric.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The energy relaxation time T_1 of superconducting qubits is affected by dielectric loss, non-equilibrium quasiparticles [1], and charge or bias noise, and varies between a few nano- and several microseconds, depending on qubit type, material, and device layout. Superconducting qubits are commonly based on Al thin films, and their central element, the nonlinear inductor given by a Josephson tunnel junction (JJ), is formed either by overlap [2] or by window-type geometries [3]. Qubit spectroscopy reveals coupling to stochastically distributed two-level systems (TLSs) in the tunnel oxide [4–8] which provides a channel for qubit decoherence. While the physical nature of the TLSs is still under debate, their number was shown to decrease with junction size and their density with higher atomic coordination number of the tunnel oxide [3, 9]. The number of coherent oscillations in the qubit is limited by, among other decoherence mechanisms such as non-equilibrium quasiparticles, the effective dielectric loss tangent $\tan \delta_{\text{eff}}$ [9]. The overlap geometry provides JJs with amorphous

barriers with no need for isolation dielectrics, being itself a source for additional TLSs and dielectric losses. The window geometry is used for higher quality, e.g. epitaxial, trilayer JJs with *in situ* grown barriers. Besides complex fabrication, they have the drawback of requiring additional isolation dielectrics [10]. The importance of keeping the total dielectric volume in qubits small to reduce the additional loss was shown in [9].

In this paper we give an overview of our standard technology for junction fabrication, and present an alternative junction based on sputtered trilayer stacks, which provide an intrinsically cleaner tunnel oxide and are well suited for micron-sized trilayer qubit junctions. The so-called side-wall passivated JJs provide contact to the top electrode without adding too much lossy dielectric to the circuitry, which would negatively affect the loss tangent. The trilayer isolation is achieved via an electrolytic process. These novel JJs were realized in a flux-biased phase qubit and characterized by (i) current transport measurements on reference junctions and (ii) spectroscopy and time-domain measurements of the qubit.

By systematically replacing only the Josephson junction, which is central to any superconducting qubit, we aim to analyze the loss contributions of this specific element, and, ideally, develop low-loss Josephson junctions for superconducting qubits and improve our qubit performance. We found performance comparable to the current generation of overlap phase qubits.

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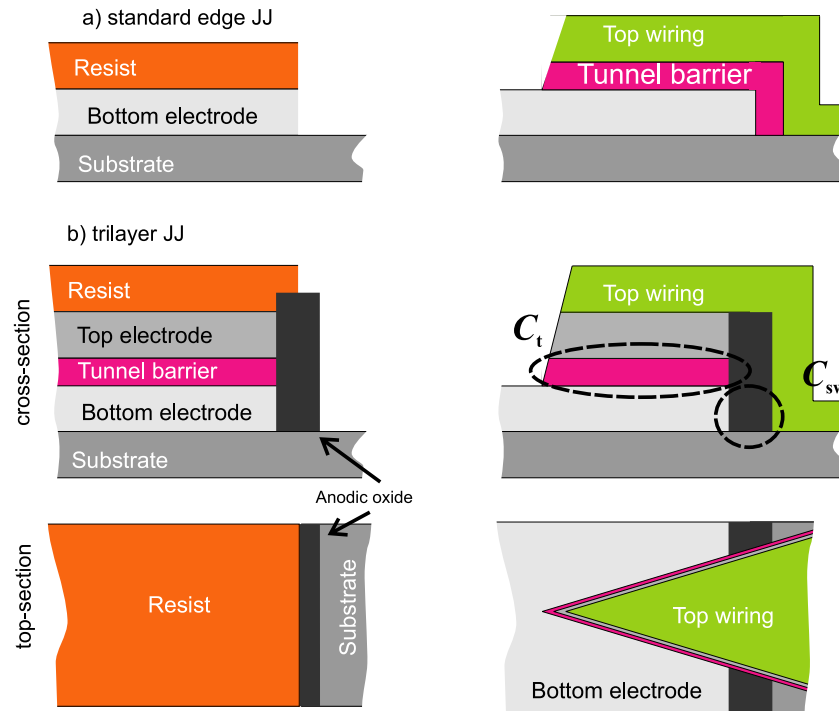


Figure 1. Schematics of (a) the overlap JJ and (b) the side-wall passivated JJ, offering minimal volume of the passivation region. Left (right) part: before (after) the top-layer deposition. After the edge etch in the trilayer stack, the side-wall oxide is grown by anodic oxidation. The trilayer JJ has *in situ* grown tunnel oxides to avoid sources of residual impurities. Patterning of the top wiring and etching below the tunnel barrier yield the tunnel junction.

2. Novel geometry

Figure 1 depicts the patterning process for our standard overlap (a) and trilayer junctions (b). Our standard process has an oxide layer grown on an ion mill cleaned aluminum edge, which was previously chlorine etched. The top wiring is then etched back below the oxide layer using argon with $\sim 10\%$ chlorine mixture. For the trilayer process, the *in situ* sputtered Al–AlO_x–Al trilayer has a thermally grown tunnel oxide barrier, formed for 10 min at 140 mTorr at room temperature. After deposition of the trilayer stack an edge is etched. The bottom electrode of the trilayer stack is isolated from the top electrode wiring by a self-aligned nanometer thin dielectric layer, grown for Al (or other suitable electrode metals such as Nb) by anodic oxidation [11]. The metallic aluminum serves as a partly submerged anode in a liquid electrolytic mixture of 156 g ammonium pentaborate, 1120 ml ethylene glycol and 760 ml H₂O at room temperature. A gold-covered metal served as cathode and the electric contact was made outside the electrolyte to the anode. By protecting parts of the aluminum electrode with photoresist only a well-defined area was oxidized by passing a constant current through the Al film and converting the metallic surface to its oxide form. The oxide thickness can be controlled by the voltage drop across the electrolyte. After a light ion clean and top wiring deposition the resist is patterned to define the junction area. Finally, the trilayer is etched below the tunnel barrier, yielding Josephson junctions with planar tunnel barrier and isolation dielectric on just one side of the tunnel area. For Nb junctions

a similar patterning process, without minimizing the dielectric loss contribution, was developed using anodic Nb oxide and covered by SiO₂ [12]. The *in situ* grown tunnel oxide avoids sources of residual impurities such as hydrogen, hydroxide or carbon at the interface vicinity, which may remain even after ion-milling in our standard process. These trilayer junctions are fully compatible with our standard process using overlap patterning and no junction side-wall.

2.1. Transport

Transport measurements on a $\sim 3 \mu\text{m}^2$ reference junction at 100 mK are shown in figure 2. The critical current I_c is $1.80 \mu\text{A}$, with normal resistance $R_n = 150 \Omega$, yielding $I_c R_n = 270 \mu\text{V}$, close to the calculated Ambegaokar–Baratoff value of $I_c R_n = 298 \mu\text{V}$ for the measured superconducting gap of $190 \mu\text{V}$. The back bending of the voltage close to the gap voltage is attributed to self-heating inside the junction. The retrapping current of $\approx 0.01 \times I_c$ indicates a very small subgap current. The current transport is consistent with tunneling, and we can exclude transport via metallic pinholes, located in the $\sim 5 \text{ nm}$ thin side-wall dielectric. As a further check, the $I_c(T)$ dependence is as expected, see inset in figure 2, with a critical temperature T_c of 1.2 K.

3. Measurement

The qubit is a flux-biased phase qubit that is coupled via a tunable mutual inductance to the readout-SQUID [13]. The

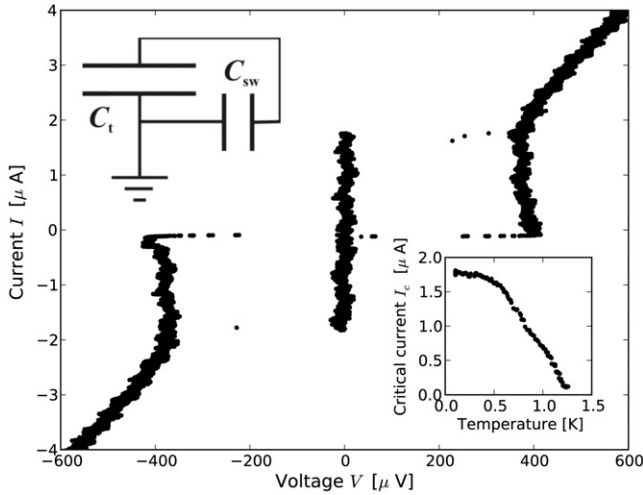


Figure 2. Current–voltage characteristic at 100 mK and $I_c(T)$ dependence (lower inset) of a $3 \mu\text{m}^2$ side-wall passivated trilayer junction. Top inset: dielectric circuit elements of the junction. The tunnel oxide capacitance C_t is connected in parallel with the capacitor formed by the side-wall oxide C_{sw} .

total qubit capacitance C_{total} , see upper inset of figure 3, is given by the tunnel oxide C_t , the anodic side-wall oxide C_{sw} and the shunt capacitor $C_s \approx 1250$ fF dielectric, provided by a parallel plate capacitor with relative permittivity $\epsilon' \approx 11.8$, made from hydrogenated amorphous silicon (a-Si:H). The measurement process follows the standard phase qubit characterization [14].

3.1. Spectroscopy

When operated as a qubit, spectroscopy over a range of more than 2.5 GHz revealed clean qubit resonance spectra with just two avoided level crossings of 40–50 MHz coupling strength (at 6.96 and 7.32 GHz, as shown in figure 3). The excitation pulse length is $1 \mu\text{s}$, and the qubit linewidth is about 3 MHz in the weak power limit. The qubit visibility, measured in a separate experiment, is about 86%, which is in the range we found for our standard phase qubits.

Qualitatively, the TLS number and coupling strength per qubit are lower than in other trilayer systems [3] that have larger tunnel areas. The TLS density per qubit has roughly the same order of magnitude as in conventional overlap qubits with similar tunnel area dimensions [2].

3.2. Relaxation

Qubit relaxation measurements via π pulse excitation and time-varied delay before readout pulse were obtained when operated outside the avoided level structures. We measured a relaxation time T_1 of about 400 ns, as shown in the lower inset of figure 3. This relaxation time is similar to that observed in the overlap qubits, which consistently have 300–500 ns for $\sim 2\text{--}4 \mu\text{m}^2$ JJ size. Apart from the change to trilayer junctions, no modification from the previous design was made.

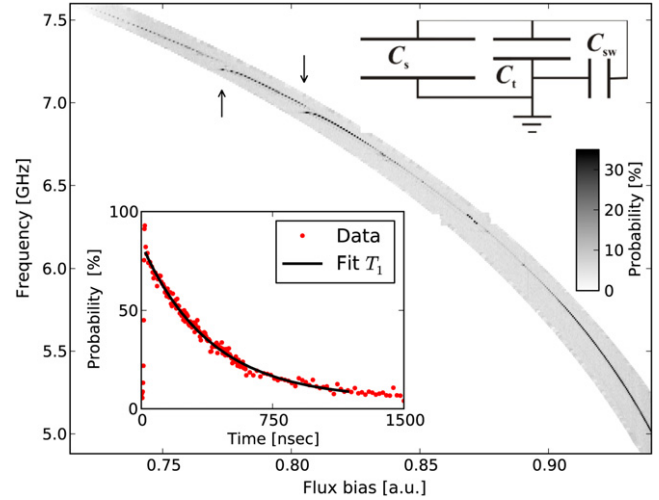


Figure 3. 2D spectroscopy of a side-wall passivated trilayer qubit at 25 mK. Two avoided level crossings due to qubit–TLS coupling are observed at 6.96 and 7.32 GHz (arrows). Top inset: dielectric circuit schematics of the qubit. Bottom inset: qubit relaxation measurement.

4. Loss estimation

We estimate the additional dielectric loss due to the side-wall oxide. The effective loss tangent of a parallel combination of capacitors is given by

$$\tan \delta_{\text{eff}} = \frac{\epsilon''_{\text{eff}}}{\epsilon'_{\text{eff}}} = \frac{\sum_i \epsilon''_i \frac{A_i}{d_i}}{\sum_i \epsilon'_i \frac{A_i}{d_i}} = \frac{\sum_i C_i \tan \delta_i}{\sum_i C_i}$$

with ϵ'_i and ϵ''_i being the real and imaginary parts of the individual permittivity for capacitor i with area A_i and dielectric thickness d_i .

Now, we discuss the individual loss contributions for all dielectrics. We design the qubit so that the dominant capacitance comes from the shunt capacitor made from a-Si:H, which has a relatively low loss tangent of 2×10^{-5} . Including the non-negligible capacitance of the tunnel junction, this gives an effective loss tangent to the qubit of 1.83×10^{-5} . Because the junction capacitance is about 10% of the shunting capacitance, the effective junction loss tangent is ten times less than the loss tangent of the junction oxide. We statistically avoid the effects of two-level systems by purposely choosing to bias the devices away from the deleterious resonances. The loss tangent of the junction is smaller than the value for bulk aluminum oxide, approximately 1.6×10^{-3} , and probably smaller than 5×10^{-5} , since long energy decay times (500 ns) have been observed for an unshunted junction when operated away from resonances [9].

The anodic side-wall oxide contributes a small capacitance of about 3.2 fF, which can be calculated assuming a parallel plate geometry. Here, we use the dielectric constant $\epsilon' = 9$ for aluminum oxide, assume an area given by $2 \mu\text{m}$, the width of the overlap, multiplied by $0.1 \mu\text{m}$, the thickness of the base layer, and estimate the thickness of the oxide as $\simeq 5$ nm, as determined by the anodic process [11]. The anodic oxide is assumed to have a bulk loss tangent of 1.6×10^{-3} [15], which

Table 1. Dielectric parameters for anodic oxide, shunt capacitance, and tunnel barrier. $\tan \delta$ is given for low temperature and low power at microwave frequencies. The capacitance for the tunnel oxide AlO_x is taken and corrected for Al electrodes from [16] for the dimensions given in the text. For qubits the loss tangent is calculated away from TLS resonances, as the losses in the small size anodic side-wall oxide and tunnel barrier are smaller than the bulk value considered for the specific loss contribution $\frac{C_i}{C_{\text{total}}} \tan \delta_i$. The measured loss $\tan \delta_m$ is a factor 3 smaller than $\tan \delta_{\text{eff}}$, the weighted sum of all specific loss contributions.

Dielectric elements	Capacitance (fF)	Loss, $\tan \delta_i$	$\frac{C_i}{C_{\text{total}}} \tan \delta_i$
Shunt capacitor a-Si:H	C_s 1250	2×10^{-5}	1.83×10^{-5} [15]
Anodic side-wall oxide	C_{sw} 3.2	$<1.6 \times 10^{-3}$	$<3.7 \times 10^{-6}$ [9]
Tunnel barrier	C_t 116	$<1.6 \times 10^{-3}$	$<1.36 \times 10^{-4}$ [9]
Measured $\tan \delta_m$			6.6×10^{-5}

gives a net qubit loss contribution of 3.7×10^{-6} , about five times lower than for the a-Si:H capacitor. Note that we expect the loss from this capacitance to be even lower because of statistical avoidance of the TLS loss [9]. The small volume of the capacitor, equivalent to a $\sim 0.5 \mu\text{m}^2$ volume tunnel junction, implies that most biases do not put the qubit on resonance with two-level systems in the anodic oxide.

5. Qubit lifetime and effective loss tangent

From the measured energy decay time, $T_1 = 400$ ns, we determine the loss tangent of the qubit to be $\delta_m = (T_1 \omega_{10})^{-1} \approx 6.6 \times 10^{-5}$, using a qubit frequency of $\omega_{10}/2\pi = 6$ GHz. This is 3 times larger than our estimation of our dielectric losses, as shown in table 1. We believe the qubit dissipation mechanism comes from some other energy loss sources as well, such as non-equilibrium quasiparticles [1].

6. Conclusion

In conclusion, we have shown that the use of an anodic oxide, self-aligned to the junction edge, does not degrade the coherence of the present phase qubits [14]. We found performance comparable to the current generation of overlap phase qubits.

The new junction geometry may provide a method to integrate submicron sized, superior quality junctions (lower TLS densities) grown, for example, by MBE epitaxy to eliminate the need for shunt dielectrics. Also, our nanometer thin, three-dimensional conformal anodic passivation layer can be replaced by a self-aligned isolation dielectric at the side-wall, which could be used for all types of trilayer stacks.

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